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(71) Applicant *(for all designated States except US)*: MAXIM INTEGRATED PRODUCTS, INC. [US/US]; 120 San Gabriel Drive, Sunnyvale, CA 94086 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: LEE, Sheng-Hann [US/US]; 14029 Saratoga Hills Road, Saratoga, CA 95070 (US).

(74) Agent: BLAKELY, Roger, W.; Blakely, Sokoloff, Taylor & Zafman, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

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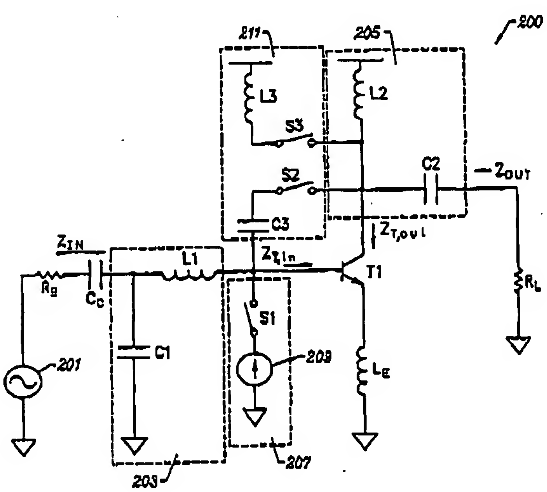
(54) Title: LOW-LOSS BYPASS MODE OF AN AMPLIFIER WITH HIGH LINEARITY AND MATCHED IMPEDANCE




(57) Abstract: A switchable gain amplifier is provided. The amplifier includes an input, an output, and a first transistor having a control region, a first region, and a second region. The conduction from the first region to the second region of the first transistor is responsive to the voltage on the control region relative to the second region. An input impedance matching network is coupled with the input and the control region and an output impedance matching network is coupled with the output and the first region. A first switchable biasing circuit is coupled with the control region to switchably bias the transistor between an on state and an off state. A passive bypasse network has a firt switch to switchably couple the input impedance matching network with the output impedance matching network through the passive bypass network.

WO 02/15397 A2

# LOW-LOSS BYPASS MODE OF AN AMPLIFIER WITH HIGH LINEARITY AND MATCHED IMPEDANCE

## BACKGROUND OF THE INVENTION

The invention relates to electronic circuits. In particular, the invention relates to radio frequency amplifiers with high linearity.

In a typical radio, signals received by an antenna are fed to a low noise amplifier (LNA) in order to amplify the received signal and thus improve the radio's receiving sensitivity. Radios to be used with the communication standard known as Code-Division-Multiple-Access (CDMA), however, present some additional challenges. For instance, as is well known in the art, a LNA to be used in CDMA systems must have a high sensitivity. In order to achieve the high sensitivity required, the LNA must provide high gain for receiving weak signals, while also maintaining high linearity. But when a LNA operates with high gain, interfering signals, including the radio's own transmitted signal, may cause the LNA to operate outside of its linear range, thus reducing the radio's sensitivity. Additionally, in order to achieve the requisite linearity, a LNA must typically be biased with a high direct current (DC) bias current. However, CDMA radios are usually powered with batteries. The high bias current required by the LNA reduces battery life and time between recharging, which are often critical design criteria in mobile radios.

Tests with CDMA radios in operation show that the high gain provided by a typical LNA is needed only a minority of the time. Most of the time, the strength of the received signal is such that a low gain is sufficient to provide the requisite receiver sensitivity. Therefore, circuit designers have sought LNAs that may be switched to one or more lower gain modes when high gain is not required. When a LNA is operated at a lower gain, interference signals have less of a deleterious effect on the LNA's linearity. Additionally, less power is consumed at lower gains, thus improving battery life.

However, the design of a LNA that may be switched between a high gain mode and a low gain mode is further constrained by impedance matching requirements, as will be discussed with reference to Fig. 1. Fig. 1 illustrates a portion of the transmit and receive paths of a typical CDMA radio. An antenna 101 both receives and transmits radio frequency (RF) signals for the CDMA radio, and is coupled to a filter 103, which is in turn coupled to a duplexer 105. CDMA is a full-duplex communications protocol, and

the duplexer 105 is employed to prevent the radio's transmit signals from interfering with the received signals and overloading the receiver. The duplexer 105 operates in a manner well known in the art to isolate the radio's receive path from its transmit path.

As seen in Fig. 1, the received signal output of the duplexer 105 is fed to the LNA 107. The isolation performance of a duplexer is dependent upon proper impedance matching between the output impedance of the duplexer 105 and the input impedance of the LNA 107. For example, manufacturers of duplexers often specify a range in which the input impedance of an interfacing circuit must fall in order to guarantee a specified isolation performance. If the input impedance of the interfacing circuit falls outside of this range, the performance of the duplexer is degraded. Therefore, when the input impedance of the LNA 107 is not adequately matched with the output impedance of the duplexer 105, more transmit signal is leaked into the receive path, degrading the performance of the receiver. The output of the LNA 107 is fed to an image rejection filter 109 which filters the received signal in a well known manner. As with the duplexer 105, the performance of the image rejection filter (IRF) 109 is dependent upon proper impedance matching between the output impedance of the LNA 107 and the input impedance of the IRF 109. Thus, improper matching of the LNA's output impedance will also degrade the performance of the receiver.

Fig. 2 illustrates one prior attempt to address some of the above discussed problems. The amplification circuit 120 of Fig. 2 may be switched between two gain modes as will be discussed below. By switching the amplifier 120 into a lower-gain mode, non-linearity caused by interfering signals is reduced and less power is consumed. When switch S1 is open, the amplifier is in a high gain mode. In the high gain mode, inductor L1 and capacitor C1 act to transform the input impedance of the amplifier circuit 120 such that $Z_{IN}$ approximates impedance $R_S$ of the duplexer 105 (the duplexer 105 is represented in Fig. 2 as signal source 125 in series with resistor $R_S$). Similarly, L2 and C2 act to transform the output impedance of the amplifier circuit 120 such that $Z_{OUT}$ approximates impedance $R_L$ of the image rejection filter 109 (the image rejection filter 109 is represented in Fig. 2 as resistor $R_L$). As is well understood to those skilled in the art, the gain of the amplifier circuit 120 in high-gain mode is determined, in part, by the value of inductor $L_E$. In general, as $L_E$ is increased, the gain of the amplifier is decreased.

The amplification circuit 120 is switched into lower-gain mode by closing switch S1. When S1 is closed, the shunt feedback capacitor C3 is included in the circuit. Shunt capacitor C3 acts to reduce the gain of the amplification circuit. In general, the

higher the value of C3, the more the gain of the circuit is reduced. However, shunt capacitor C3 also affects the input impedance $Z_{IN}$. In particular, as the value of C3 is increased, the input impedance $Z_{IN}$ of the circuit 120 is decreased. As discussed above, input impedance $Z_{IN}$ must approximate $R_S$ in order for duplexer 105 to perform optimally. Therefore, the value of C3 is constrained by its effect on the input impedance $Z_{IN}$. On the other hand, increasing the value of $L_E$ generally increases the input impedance of the circuit. Hence, $L_E$ could be increased in order to offset the decrease in input impedance caused by C3. However, as discussed above, increasing the value of $L_E$ tends to lower the gain of the circuit in high gain mode, and thus $L_E$ is also constrained. Therefore, the circuit of Fig. 2 may achieve only a limited reduction of gain in its low-gain mode without adversely affecting either the impedance match with the duplexer 105 or the gain of the circuit in high-gain mode. Additionally, the circuit 120 achieves only a modest reduction in power consumption in its low-gain mode.

Fig. 3 illustrates an improvement to the amplification circuit 120 of Fig. 2. In particular, circuit 140 provides four different gain modes as will be discussed below. The additional gain modes may be of lower gain than is achievable with the circuit of Fig. 2. The amplification circuit 140 basically comprises two amplification circuits, labeled 141 and 145, that each operate in a manner similar to the circuit of Fig. 2. As with the amplifier 120 of Fig. 2, C1 and L1 act to match $Z_{IN}$ with $R_S$, and L2 and C2 act to match $Z_{OUT}$ with $R_L$. Switches S2 and S4 are used to select which of amplification circuits 141 and 145 is active. Switches S1 and S3 operate in a manner similar to the switch S1 of Fig. 2 to switch their respective amplification circuit between high gain mode and lower gain mode. In operation, when switch S2 is closed and switches S1, S3, and S4 are open, transistor T1 is biased on and transistor T2 is biased off. In this mode, the amplification circuit 145 is essentially inactive, and the amplification circuit 141 operates in a high gain mode. Similarly, when switch S1 is closed, the gain is reduced with the inclusion of the shunt feedback capacitor C3.

When switch S4 is closed and switches S1, S2, and S3 are opened, amplification circuit 141 is biased off and amplification circuit 145 becomes active. The value of inductor L4 is chosen such that the gain of amplifier 145 in its high-gain mode is lower than that provided by either of the modes of amplification circuit 141. Additionally, when S3 is closed, shunt feedback capacitor C4 is switched into the circuit and the gain is further reduced without adversely affecting the input impedance match. Thus, the circuit 140 provides two additional lower gain levels while still providing an

acceptable input impedance match. However, this circuit provides only a modest reduction in power usage.

## SUMMARY OF THE INVENTION

According to the invention, a switchable gain amplifier is provided. The amplifier comprises an input, an output, and a first transistor having a control region, a first region, and a second region, the conduction from the first region to the second region of the first transistor being responsive to the voltage on the control region relative to the second region. The amplifier also comprises an input impedance matching network coupled with the input and the control region and an output impedance matching network coupled with the output and the first region. The amplifier further comprises a first switchable biasing circuit coupled with the control region to switchably bias the transistor between an on state and an off state, and a passive bypass network coupled with the input impedance matching network and the output impedance matching network. The passive bypass network has a first switch to switchably couple the input impedance matching network with the output impedance matching network through the passive bypass network.

In another embodiment of the invention, a method of amplifying an input signal is provided. The method includes providing an amplification circuit including an amplifying transistor and a passive bypass network. The method also includes biasing the amplifying transistor into an ON state and isolating the passive bypass network from the amplification circuit to configure the amplification circuit in an amplifier mode, wherein in the amplifier mode, an input impedance of the amplification circuit is substantially matched with a source impedance and an output impedance of the amplification circuit is substantially matched with a load impedance. The method further includes inputting the input signal to the amplification circuit in the amplifier mode to form a high-gain amplified output signal. The method also includes biasing the amplifying transistor into an OFF state and coupling the passive bypass network into the amplification circuit to configure the amplification circuit in a bypass mode, wherein in the bypass mode, the input impedance of the amplification circuit is substantially matched with the source impedance and the output impedance of the amplification circuit is substantially matched with the load impedance. The method still further includes inputting the input signal to the amplification circuit in the bypass mode to form a low-gain amplified output signal.

In another aspect of the invention, a switch is provided for switchably coupling an input with an output. The switch comprises a first diode having an anode coupled with the output and a cathode coupled with the input. The switch also comprises a second diode having an anode coupled with the input and a cathode. The switch further comprises a first capacitor coupled with the anode of the first diode and the cathode of the second diode. The switch still further comprises a switchable current source coupled in series with the first diode and the second diode to switchably supply a bias current through the first diode and the second diode.

In yet another aspect of the invention, a method of switchably coupling an input with an output is provided. The method includes providing a switch comprising a first diode having an anode coupled with the output and a cathode coupled with the input, a second diode having an anode coupled with the input and a cathode, a first capacitor coupled with the anode of the first diode and the cathode of the second diode, and a switchable current source coupled in series with the first diode and the second diode to switchably supply a bias current through the first diode and the second diode. The method also includes switching the switchable current source to an ON state to couple the input with the output, and switching the switchable current source to an OFF state to isolate the input from the output.

Benefits of embodiments of the present invention include providing a switchable gain amplifier with increased linearity and decreased losses. Other benefits include providing a switchable gain amplifier having a lower gain in its low-gain mode while still maintaining impedance match. Further benefits include providing a switchable gain amplifier with lower power consumption. Still other benefits include providing a switch with improved linearity, improved isolation, and reduced losses.

## BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a portion of a transmit path and a receive path of a typical Code-Division-Multiple-Access (CDMA) radio;

Fig. 2 is a simplified circuit diagram of a prior art switchable gain amplifier;

Fig. 3 is a simplified circuit diagram of another prior art switchable gain amplifier;

Fig. 4 is a simplified circuit diagram of an embodiment of a switchable gain amplifier according to the invention;

Fig. 5 is a simplified alternating current (AC) equivalent circuit of the switchable gain amplifier embodiment of Fig. 4 in an amplifier mode;

Fig. 6 is a simplified AC equivalent circuit of the switchable gain amplifier embodiment of Fig. 4 in a bypass mode;

Fig. 7 is a simplified circuit diagram of another embodiment of a switchable gain amplifier according to the invention;

Fig. 8 is a simplified circuit diagram of yet another embodiment of a switchable gain amplifier according to the invention;

Fig. 9 is a simplified circuit diagram of still another embodiment of a switchable gain amplifier according to the invention;

Fig. 10 is a simplified circuit diagram of yet another embodiment of a switchable gain amplifier according to the invention;

Fig. 11 is a simplified circuit diagram of still another embodiment of a switchable gain amplifier according to the invention;

Fig. 12 is a simplified AC equivalent circuit of an embodiment of a switch according to an aspect of the invention;

Fig. 13 is a simplified circuit diagram of another embodiment of a switchable gain amplifier according to the invention; and

Fig. 14 is a simplified circuit diagram of another embodiment of a switch according to an aspect of the invention.

## DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Fig. 4 is a simplified circuit schematic that illustrates an embodiment of a switchable-gain amplifier according to the invention. An amplifier 200 is switchable between a gain mode and a bypass mode. In the gain mode, the amplifier 200 is matched with a source impedance and a load impedance, and operates in a typical manner to amplify the input signal. However, when high gain is not required, the amplifier 200 may be switched into a bypass mode. In the bypass mode, the transistor is biased off, and the input signal is routed through a passive bypass network that comprises only passive components. The passive bypass network maintains impedance matching with the source and load impedances in the bypass mode. The invention differs from the circuits illustrated in Figs. 2 and 3 in that the passive bypass network is not a feedback circuit. Rather, the passive bypass network acts to redirect the signal around the inactivated transistor. The present invention provides several advantages over amplifiers such as

those shown in Figs. 2 and 3. For example, the present invention provides improved linearity and decreased losses because, in the bypass mode, the signal is not routed through a transistor. Rather, the signal passes through a passive-only network, which exhibits very high linearity and low loss. Also, the present invention provides a significant reduction in gain in its bypass mode while maintaining proper impedance matching with the source impedance and the load impedance. Additionally, because the transistor is biased off in bypass mode, the amplifier 200 consumes only a fraction of the power required in gain mode, thus improving battery life and time between recharging in battery-powered devices.

Referring to Fig. 4, a signal source having an impedance $R_S$ is coupled with an input impedance matching network 203 of the amplifier circuit 200 through a coupling capacitor $C_C$. The input impedance matching network 203 is in turn coupled to the base of a transistor T1. The emitter of the transistor T1 is coupled with ground through an emitter inductor $L_E$. The collector of the transistor T1 is coupled with $V_{CC}$ through inductor L2. The collector of transistor T1 is also coupled with a capacitor C2 which is in turn coupled with a load $R_L$. An output impedance matching network 205 comprises inductor L2 and C2. A switchable biasing circuit 207 coupled with the base of transistor T1 comprises switch S1 and current source 209, and switchably biases transistor T1 between an ON state and an OFF state, as will be discussed below. Additionally, the amplifier circuit 200 includes a passive bypass network 211 coupled with the input impedance matching network 203 and the output impedance matching network 205. The passive bypass network 211 includes a bypass capacitor C3 coupled in series with a switch S2, and a bypass inductor L3 coupled in series with a switch S3. The amplifier 200 has an input impedance $Z_{IN}$ and an output impedance $Z_{OUT}$.

To put the amplifier 200 in gain mode, switch S1 is closed and switches S2 and S3 are opened. When switch S1 is closed, current source 209 supplies a current to a base of transistor T1, which in turn causes a bias current to flow into a collector of the transistor T1. The amount of current supplied by current source 209 is chosen such that transistor T1 operates in the gain mode with the requisite linearity. When switches S2 and S3 are opened, capacitor C3 and inductor L3 are effectively isolated from the circuit. The gain of the circuit 200 in gain mode is set in a manner well known to those skilled in the art.

Fig. 5 is a simplified alternating current (AC) equivalent circuit of the circuit shown in Fig. 4 operating in its gain mode (e.g. inductor $L_E$ has been excluded for

simplicity). Fig. 5 illustrates impedance matching of the amplifier 200 in its gain mode. Transistor T1 may be modeled as shown in Fig. 5, having a bias current-dependent input impedance $Z_{T,IN}$, as well as a bias current-dependent output impedance $Z_{T,OUT}$. Resistor $R_P$ represents combined bias current-independent parasitic losses of the transistor T1 and inductor L2. Capacitor C1 and inductor L1 comprise an input impedance matching network. In order to match the input impedance $Z_{IN}$ with $R_S$, the values of C1 and L1 are chosen in a well known manner to transform $R_S$ to $Z^*_{T,IN}$. Similarly, capacitor C2 and inductor L2 comprise an output impedance matching network. In order to match the output impedance $Z_{OUT}$ with $R_L$, the values of C2 and L2 are chosen in a well known manner to transform $R_L$ to $(Z_{T,OUT} \| R_P)^*$.

Referring again to Fig. 4, amplifier 200 may be put into a bypass mode. To put the amplifier 200 in bypass mode, switch S1 is opened and switches S2 and S3 are closed. When is S1 opened, the current from current source 209 is removed from the base of transistor T1, causing the bias current into the collector of T1 to decrease to substantially zero. When the bias current of T1 goes to zero, transistor T1 is biased OFF and is effectively removed from the circuit. When switches S2 and S3 are closed, the bypass network 211 comprising bypass capacitor C3 and bypass inductor L3, is coupled into the amplifier circuit 200. Fig. 6 is a simplified AC equivalent circuit of amplifier circuit 200 operating in its bypass mode. In the bypass mode, the input impedance matching network is coupled with the output impedance matching network via the bypass network. The values of C3 and L3 are chosen in a well known manner to match $R_S$ and $R_L$.

Fig. 7 illustrates another embodiment of the invention. Amplifier circuit 250 is similar to the circuit 200 of Fig. 4, except that the passive bypass network 211 no longer includes inductor L3 nor switch S3. Amplifier circuit 250 operates in the same manner as the circuit 200 of Fig. 4. However, in bypass mode, a perfect impedance match cannot be achieved because only the bypass capacitor C3 is available for impedance transformation. It has been found that an acceptable, though imperfect, impedance match may still be achieved with only the bypass capacitor C3. In particular, the value of L2 may be reduced to a value where the output impedance match in the gain mode, though not ideal, is nevertheless acceptable, and where the impedance match in the bypass mode, though also not ideal, is also acceptable. This may be explained with reference to Fig. 6. Fig. 6 shows the simplified AC equivalent of circuit 200 in the bypass mode, which includes bypass inductor L3. As can be seen, bypass inductor L3 is

connected in parallel with inductor L2. Thus, when inductor L3 is included in the circuit 200 in bypass-mode, it acts to reduce the value of the inductor L2. Basically, in the bypass mode, the value of L2 is changed to L2 , where L2 = L2 || L3.

Referring to Figs. 4 and 7, the circuit 250 provides a cost savings over the circuit 200 at the expense of less-than-ideal impedance matching. In particular, circuit 250 eliminates inductor element L3. In general, inductors cannot easily be integrated onto an integrated circuit (IC) and are relatively expensive components.

Fig. 8 illustrates another embodiment of the invention. A circuit 270 is similar to the circuit 250 of Fig. 7, except that passive bypass network 211 includes resistor R3 and switch S3 for improving impedance match in the bypass mode. In operation, switch S1 is closed during amplifier mode, and switches S2 and S3 are opened to isolate capacitor C3 and resistor R3 from the circuit. In amplification mode, circuit 270 operates in a similar manner to circuit 200 of Fig. 4 and circuit 250 of Fig. 7 in their respective amplifier modes. In a bypass mode of circuit 270, switch S1 is opened to remove transistor T1 from the circuit as discussed previously. Switches S2 and S3 are closed so that capacitor C3 and resistor R3 are included in the circuit. The resistor R3 acts as a shunt attenuator in the bypass mode, and may provide an improvement in impedance match over the circuit 250 of Fig. 7 in a manner well known in the art. Although a perfect impedance match cannot be obtained using the resistor R3, using a resistor is less expensive than using inductor L3 of Fig. 4. Additionally, the resistor R3 may be easily integrated onto an IC with other components of the circuit 270, unlike the inductor L3 of Fig. 4. Resistor R3 does, however, increase the loss in the circuit 270 in bypass mode. But, in general, the loss introduced by R3 is acceptable because, as is well known in the art, signal loss is a nonlinear function of impedance match, and so the benefits resulting from the better impedance match easily outweighs the harm caused by the slightly increased loss.

Referring now to Figs. 4, 7, and 8, the switchable biasing circuit 207 for biasing transistor T1 has been symbolically shown as the current source 211 coupled in series with switch S1. However, other switchable biasing circuits may also be used. For example, in an embodiment, the separate switch S1 may be eliminated by using a switchable current source for current source 209. In another embodiment, the switchable biasing circuit 207 may comprise a switchable power source coupled in series with a resistor. Many other methods of switchably biasing a transistor known to those skilled in the art may also be used.

Switches S2 and S3 in Figs. 4, 7, and 8 should exhibit high linearity and low loss due to their position within the signal path in bypass mode. For example, the switches S2 and S3 may comprise metal oxide semiconductor (MOS) field effect transistors. Fig. 9 illustrates another embodiment of the invention. In particular, Fig. 9 shows a circuit 300, which is similar to the circuit 250 of Fig. 7, except that the switch S2 comprises a MOS transistor T2. A control signal is coupled with a gate lead of a MOS transistor T2. When the control signal is brought to an ON voltage level, a channel between a drain and source of transistor T2 becomes conductive and capacitor C3 is effectively switched into the circuit 300. When the control signal is brought to an OFF voltage level, the drain and source of transistor T2 become electrically isolated from each other, and the capacitor C3 is effectively switched out of the circuit 300. Using a MOS transistor for switches S2 and S3 has several advantages. For instance, in a conductive state, the channel between the drain and source of a MOS transistor exhibits very good linearity. Also, a MOS transistor switch consumes substantially no power. However, it may be impractical to use a MOS transistor for switches S2 and S3 unless the amplifier circuit 300 is to be implemented using a BiCMOS fabrication process. Additionally, MOS transistors are relatively lossy as compared to bipolar transistors of approximately the same size. Thus, a switch comprising a MOS transistor may consume a relatively large amount of IC area in order to reduce loss to an acceptable level.

Fig. 10 illustrates yet another embodiment of the invention. In Fig. 10, the switch S2 comprises a diode D1 coupled with a switchable current source 351. In particular, an anode of D1 is coupled with the inductor L2, capacitor C2, and the collector of transistor T1. The cathode of D1 is coupled with the capacitor C3. Switchable current source 351 is coupled with the cathode of D1. In operation, when the switchable current source 351 is switched ON, it draws a bias current through diode D1. The bias current causes D1 to become conductive, and thus C3 is switched into the circuit 350. When the switchable current source 351 is switched OFF and the bias current no longer flows through diode D1, the impedance of D1 becomes extremely high and capacitor C3 is isolated from inductor L2, capacitor C2, and transistor T1. However, the diode switch illustrated in Fig. 10 has a drawback—its linearity. In particular, the illustrated diode switch has relatively poor linearity because of two well known properties of diodes. First, the impedance of the diode is dependent upon the current through the diode. Second, the impedance of the diode D1 is not symmetrical as the current through the diode D1 swings

about the bias current. The asymmetry of the impedance substantially degrades the linearity of the switch.

Fig. 11 illustrates still another embodiment of the invention that provides an improvement in linearity. In this embodiment, a cathode of a diode D1 is coupled with capacitor C3, and an anode of diode D1 is coupled with inductor L2, capacitor C2, and the collector of transistor T1. An anode of a second diode D2 is coupled with the cathode of diode D1, and a cathode of diode D2 is coupled with the switchable current source 351. A coupling capacitor C4 is coupled between the anode of D1 and the cathode of D2. In operation, when the switchable current source 351 is switched ON, it draws a bias current through diodes D1 and D2. The bias current causes diodes D1 and D2 to become conductive, and thus, C3 becomes coupled to the collector of T1 through two parallel paths. When the switchable current source 351 is switched OFF and the bias current no longer flows through diodes D1 and D2, their respective impedances become extremely high and capacitor C3 is isolated from the circuit 400.

The circuit 400 provides several improvements over the circuit 350 of Fig. 10, as will be explained with reference to Fig. 12. Fig. 12 illustrates a simplified AC equivalent circuit of the switch S2 of Fig. 11. Because of the anode-to-cathode configuration of the diodes D1 and D2 in circuit 400, the effects of the current on each of their impedances tend to offset each other. For example, as the impedance of one diode begins to rise, the impedance of the other diode begins to fall. And, because the two diodes are connected in parallel, the change in the impedance of diode D1 with current tends to offset the change in the impedance of diode D2. Thus, the dependence of the overall impedance of the switch S2 on current is reduced. Additionally, the asymmetry of the impedance is eliminated. Hence, the linearity is improved with respect to the switch S2 of Fig. 10. Moreover, because the two diodes D1 and D2 are connected in parallel, the current through the switch S2 is effectively split evenly between the two diodes. Thus, each of the diodes D1 and D2 sees approximately one half of the current swings about the bias current as is seen by the diode in the single diode switch of Fig. 10. Therefore, the amount bias current supplied by switchable current source 351 may be kept below the amount required of the embodiment of S2 shown in Fig. 10.

Referring now to Fig. 11, drawbacks exists in using the diode switch as shown. In particular, relatively large swings in voltage occurring at the collector of transistor T1 while circuit 400 operates in the amplifier mode may cause diodes D1 and D2 to become forward biased, and thus turn ON. This will cause distortions and thus

lower the performance of the circuit 400. Additionally, in a typical switchable current source 351, the current does not go completely to zero in the current source's OFF state. Therefore, the diode switch S2 will not completely isolate capacitor C3 from the collector of transistor T1, and, hence, result in distortion and decreased performance.

It is well known in the art that diodes may be simulated using appropriately configured transistors. Numerous such configurations are known to those skilled in the art. Hence, a diode switch, such as the diode switch illustrated in Fig. 11, may be implemented using transistors configured to simulate diodes.

Fig. 13 illustrates yet another embodiment of the invention. An amplifier circuit 500 is similar to the amplifier circuit 270 of Fig. 8, but the switches S2 and S3 are implemented using embodiments of diode switches. Referring now to the circuitry labeled S2, transistors T2 and T3 simulate diodes similar to diodes D1 and D2, respectively, of Figs. 11-13. Resistor R11 is a bleeder resistor for redirecting the leakage current of switchable current source 351 in its OFF state. Resistor R13 along with switchable current source 361 act to reverse bias transistor-diode T3 when the switch S2 is in its OFF state. Similarly, resistor R17 along with switchable current source 371 act to reverse bias transistor-diode T2 in the OFF state of switch S2. Resistors R15 and R19 provide signal isolation. In particular, resistors R15 and R19 increase the impedance into the current sources 361 and 371, respectively, to reduce the amount of the amplified signal that leaks through the switches 361 and 371 when the amplifier is in high-gain mode. In operation, when switch S2 is OFF, current source 351 is switched OFF, while current sources 361 and 371 are switched ON. Resistor R11 sources the leakage current of current source 351. Thus, as previously discussed, the leakage current does not flow through transistors T2 and T3, thus improving the switch's isolation in its OFF state. R11 also pulls the voltage at the emitter of transistor T3 to near $V_{CC}$. Current source 361 and resistor R13 pull the voltage of the base of T3 to a voltage below that of its emitter, thus reverse biasing T3. Similarly, current source 371 and resistor R17 pull the voltage of the base of T2 below that of the base of T3, which is coupled to the emitter of T2. Hence, T2 is also reverse biased. Because the transistors T2 and T3 are reversed biased, large swings in voltage at the collector of T1 will not cause T2 and T3 to turn ON. Additionally, the reverse biasing of transistors T2 and T3 further improves the isolation of the switch in its OFF state, because, as is well known in the art, the respective junction capacitances of transistors T2 and T3 are reduced.

In the ON state of switch S2, current source 351 is switched ON while current sources 361 and 371 are switched OFF. Coupling capacitor C5 effectively becomes a short circuit, and resistors R11, R13, R15, R17, and R19 are effectively removed from the circuit with regard to AC signals. Thus, the S2 circuitry behaves similar to the diode switch as described with respect to Figs. 11 and 12.

Referring now to the circuitry labeled S3, another embodiment of a switch is shown for switchably connecting resistor R3 to ground. Transistors T4 and T5 simulate diodes similar to diodes D1 and D2, respectively, of Figs. 11 and 12. Capacitor C6 acts in a manner similar to that of capacitor C4 in Figs. 11 and 12. Resistors R21 and R23, together, act in a manner similar to that of the bleeder resistor R11 in Fig. 13 to sink the leakage current of the switchable current source 381 in its OFF state. Capacitor C7 acts as a coupling capacitor, and is effectively a short circuit to AC signals.

Fig. 14 illustrates yet another embodiment of a switch according to the invention. A switch 600 includes a first port 601 and a second port 603. The switch 600 switchably couples the first port 601 with the second port 603. Transistors T6 and T7 simulate diodes similar to diodes D1 and D2, respectively, of Figs. 11 and 12. Capacitor $C_{10}$ acts in a manner similar to that of capacitor C4 in Figs. 11 and 12. Resistor R31 couples the base of transistor T6 with its collector, making T6 inductive when the operating signal of the signal to be switched through switch 600 is much greater than $f_T/\beta$. Similarly, resistor R33 couples the base of transistor T7 with its collector, making T7 inductive. Thus, transistors T6 and T7 are configured to simulate diodes, with their respective collectors as anodes and their respective collectors as cathodes.

Transistor/diodes T6 and T7 are coupled in series and a switchable current source 605 is coupled with the emitter of transistor T7. The switchable current source 605 switchably biases the transistor/diodes T6 and T7 ON and OFF, similar to the switchable current source 351 of Figs. 11 and 13, and current source 381 of Fig. 13. Capacitors C10 and C11 block DC signals and are substantially short circuits to the signal to be switched through the switch 600. The values of resistors R31 and R33 and capacitor C10 are chosen in a manner well known to those skilled in the art such that the impedance comprising R33 and T7 in series with capacitor C10 are substantially the conjugate of the impedance comprising R31 and T6.

In operation, when switchable current source 605 is OFF, transistor/diodes T6 and T7 are OFF, and hence node 601 is isolated from node 603. When switchable current source 605 is switched ON, a bias current is drawn through transistor/diodes T6

and T7, making them conductive. Because of the values chosen for R31, R33, and C10 discussed above, an AC current flowing from node 601 to 603 is approximately evenly divided between a flow into the collector of T6 and a flow into the emitter of T7. Similarly, an AC current flowing from node 603 to node 601 is approximately evenly divided between a flow into the emitter of T6 and a flow into the collector of T7.

Although the above description has been described with respect to a common-emitter amplifier, the invention is not so limited. For example, the invention may be applied to other types of one-transistor amplifiers such as common-base, common collector, and the like. Additionally, the invention may be applied to multiple transistor amplifiers. Also, although the above description has been described with respect to a bipolar transistor amplifier, the invention may be applied to amplifiers including other types of transistors, such as MOS transistors and the like.

The invention has now been explained with reference to specific embodiments. Other embodiments will be apparent to those of ordinary skill in the art. Therefore it is not intended that this invention be limited except as indicated by the appended claims.

WHAT IS CLAIMED IS:

1. A switchable gain amplifier, comprising:

an input port;

an output port;

an amplifier circuit, having an amplifier circuit input and an amplifier circuit output;

a first switchable biasing circuit coupled with the amplifier circuit to switchably bias the amplifier circuit between an on state and an off state;

an input impedance matching network coupled with the input port and the amplifier circuit input;

an output impedance matching network coupled with the output port and the amplifier circuit output; and

a passive bypass network coupled with the input impedance matching network and the output impedance matching network, the passive bypass network having a first switch to switchably couple the input impedance matching network with the output impedance matching network through the passive bypass network.

2. The switchable gain amplifier of claim 1, wherein the amplifier circuit comprises a common-emitter amplifier.

3. The switchable gain amplifier of claim 2, wherein the common-emitter amplifier includes an inductor in series with the emitter.

4. The switchable gain amplifier of claim 1, wherein the amplifier circuit comprises at least two transistors.

5. The switchable gain amplifier of claim 1, wherein the input impedance matching network comprises an input impedance matching series inductor and an input impedance matching shunt capacitor.

6. The switchable gain amplifier of claim 1, wherein the output impedance matching network comprises an output impedance matching series capacitor and an output impedance matching shunt inductor.

7. The switchable gain amplifier of claim 1, wherein the passive bypass network includes a series bypass capacitor coupled with the first switch.

8. The switchable gain amplifier of claim 7, wherein the passive bypass network includes a shunt bypass inductor coupled in series with a second switch to switchably couple the shunt bypass inductor with the series bypass capacitor.

9. The switchable gain amplifier of claim 7, wherein the passive bypass network includes a shunt bypass resistor coupled in series with a second switch to switchably couple the shunt bypass resistor with the series bypass capacitor.

10. The switchable gain amplifier of claim 1, wherein the first switch comprises a MOS transistor.

11. The switchable gain amplifier of claim 1, wherein the first switch comprises a first diode having an anode coupled with the output impedance matching network and a cathode coupled with the passive bypass network, and a second switchable biasing circuit coupled with the first diode to switchably bias the first diode between an on state and an off state.

12. The switchable gain amplifier of claim 11 wherein the second switchable biasing circuit comprises a variable current source coupled with the cathode of the first diode.

13. The switchable gain amplifier of claim 11 wherein the first switch further comprises a second diode having an anode coupled with the cathode of the first diode, and a first switch capacitor coupled between the anode of the first diode and a cathode of the second diode.

14. The switchable gain amplifier of claim 13 wherein the second switchable biasing circuit comprises a variable current source coupled with the cathode of the second diode.

15. The switchable gain amplifier of claim 1, wherein the first switch comprises:

a first transistor having a control region, a first region, and a second region, the conduction from the first region to the second region of the first transistor being responsive to the voltage on the control region relative to the second region, the control region of the first transistor coupled with the first region of the first transistor and

the output impedance matching network, and the second region of the first transistor coupled with the passive bypass network;

a second transistor having a control region, a first region, and a second region, the conduction from the first region to the second region of the second transistor being responsive to the voltage on the control region relative to the second region, the control region of the second transistor coupled with the first region of the second transistor and the second region of the first transistor;

a first switch capacitor coupled between the first region of the first transistor and the second region of the second transistor; and

a second switchable biasing circuit coupled with the first and second transistors to switchably bias the first and second transistors between respective on states and respective off states.

16. The switchable gain amplifier of claim 15, wherein the second switchable biasing circuit comprises a first variable current source coupled with the second region of the second transistor.

17. The switchable gain amplifier of claim 16, wherein the second switchable biasing circuit further comprises:

a second switch capacitor coupled between the control region of the first transistor and the first region of the first transistor;

a first switch resistor coupled between the second region of the second transistor and a reference voltage;

a second switch resistor coupled between the control region of the first transistor and the first region of the first transistor;

a third switch resistor coupled between the control region of the first transistor and a second variable current source;

a fourth switch resistor coupled between the reference voltage and the control region of the second transistor; and

a fifth switch resistor coupled between the control region of the second transistor and a third variable current source.

18. A method of amplifying an input signal, the method comprising:

providing a switchable gain amplifier circuit including an amplifying circuit and a passive bypass network;

biasing the amplifying circuit into an ON state and isolating the passive bypass network from the switchable gain amplifier circuit to configure the switchable gain amplifier circuit in an amplifier mode, wherein in the amplifier mode, an input impedance of the switchable gain amplifier circuit is substantially matched with a source impedance and an output impedance of the switchable gain amplifier circuit is substantially matched with a load impedance;

inputting the input signal to the switchable gain amplifier circuit in the amplifier mode to form a high-gain amplified output signal;

biasing the amplifying circuit into an OFF state and coupling the passive bypass network into the switchable gain amplifier circuit to configure the switchable gain amplifier circuit in a bypass mode, wherein in the bypass mode, the input impedance of the switchable gain amplifier circuit is substantially matched with the source impedance and the output impedance of the switchable gain amplifier circuit is substantially matched with the load impedance; and

inputting the input signal to the switchable gain amplifier circuit in the bypass mode to form a low-gain amplified output signal.

19. The method of claim 18, wherein the amplifying circuit includes an amplifying circuit input and an amplifying circuit output, and wherein the passive bypass network comprises a capacitor coupled in series with a first switch between the amplifying circuit input and the amplifying circuit output.

20. The method of claim 19, wherein the passive bypass network further comprises an inductor coupled in series with a second switch between the amplifying circuit output and a reference voltage.

21. The method of claim 19, wherein the passive bypass network further comprises a resistor coupled in series with a second switch between the amplifying circuit input and a common voltage.

22. A switch for switchably coupling a first port with a second port, the switch comprising:

a first diode having an anode coupled with the second port and a cathode coupled with the first port;

a second diode having an anode coupled with the first port and a cathode;

a first capacitor coupled with the anode of the first diode and the cathode of the second diode; and

a switchable current source coupled in series with the first diode and the second diode to switchably supply a bias current through the first diode and the second diode.

23. The switch of claim 22 further comprising a bleeder resistor coupled between the cathode of the second diode and a reference voltage to source a leakage current of the switchable current source.

24. The switch of claim 22 wherein the first diode comprises a first transistor configured as a diode and the second diode comprises a second transistor configured as a diode.

25. The switch of claim 24 wherein the first transistor includes a control region, a first region, and a second region, the conduction from the first region to the second region of the first transistor being responsive to the voltage on the control region relative to the second region, wherein the second transistor includes a control region, a first region, and a second region, the conduction from the first region to the second region of the second transistor being responsive to the voltage on the control region relative to the second region, and wherein the switch further comprises a first resistor coupled between the first region and the control region of the first transistor, and a second resistor coupled between the first region and the control region of the second transistor.

26. The switch of claim 24 further comprising a switchable reverse biasing circuit coupled with the first and second transistors to switchably reverse bias the first and second transistors.

27. A method of switchably coupling a first port with a second port, the method comprising:

providing a switch comprising:

first diode having an anode coupled with the second port and a cathode coupled with the first port,

a second diode having an anode coupled with the first port and a cathode;

a first capacitor coupled with the anode of the first diode and the cathode of the second diode; and

a switchable current source coupled in series with the first diode and the second diode to switchably supply a bias current through the first diode and the second diode;

switching the switchable current source to an ON state to couple the first port with the second port; and

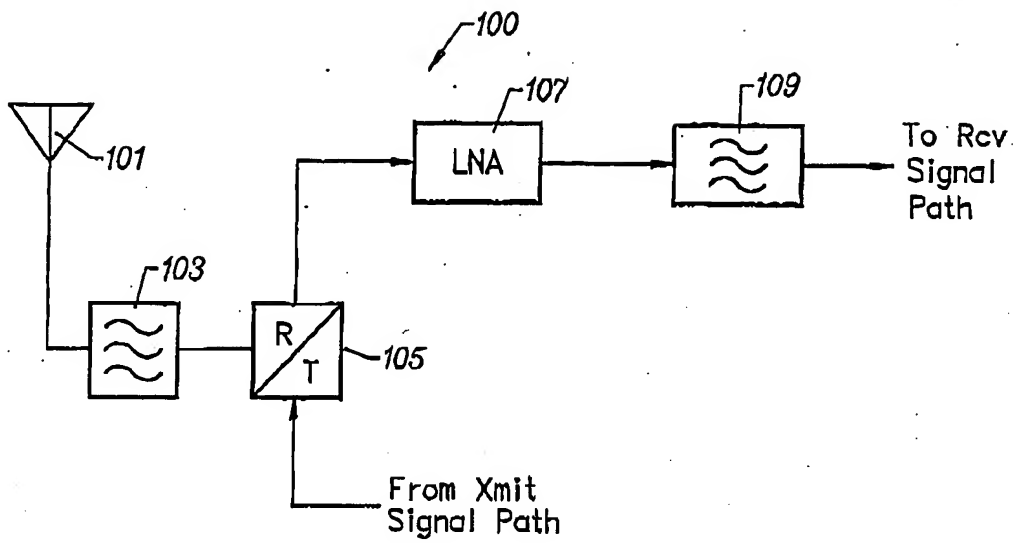
switching the switchable current source to an OFF state to isolate the first port from the second port.

28. The method of claim 27 further comprising providing a bleeder resistor coupled between the cathode of the second diode and a reference voltage to redirect a leakage current of the switchable current source in its OFF state from the first and second diodes to the bleeder resistor.

29. The method of claim 27 wherein the first diode comprises a first transistor configured as a diode and the second diode comprises a second transistor configured as a diode.

30. The method of claim 29 wherein the first transistor includes a control region, a first region, and a second region, the conduction from the first region to the second region of the first transistor being responsive to the voltage on the control region relative to the second region, wherein the second transistor includes a control region, a first region, and a second region, the conduction from the first region to the second region of the second transistor being responsive to the voltage on the control region relative to the second region, and wherein the switch further comprises a first resistor coupled between the first region and the control region of the first transistor, and a second resistor coupled between the first region and the control region of the second transistor.

31. The method of claim 29 further comprising reverse biasing the first and second transistors when the switchable current source is in its OFF state.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107
109
101
LNA
To Rcv
Signal
Path
103
R
T
105
From Xmit
Signal Path

FIG. 1

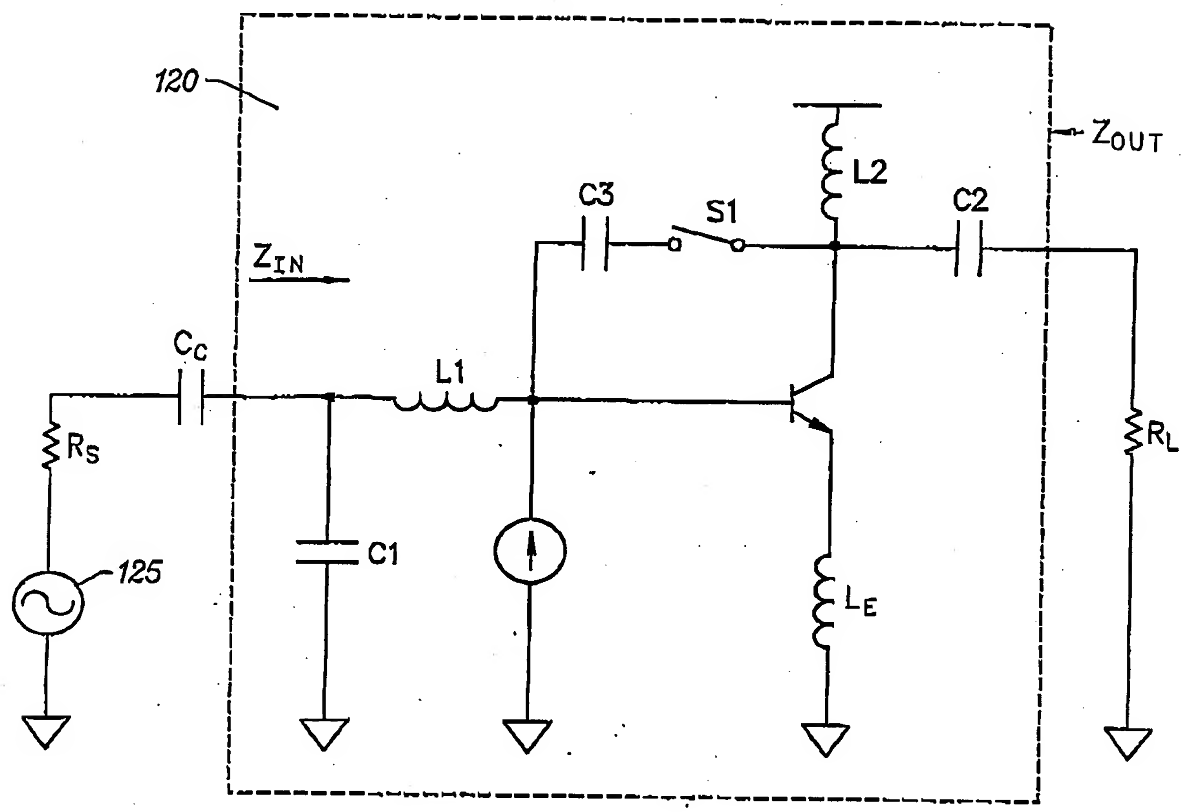



FIG. 2
(PRIOR ART)

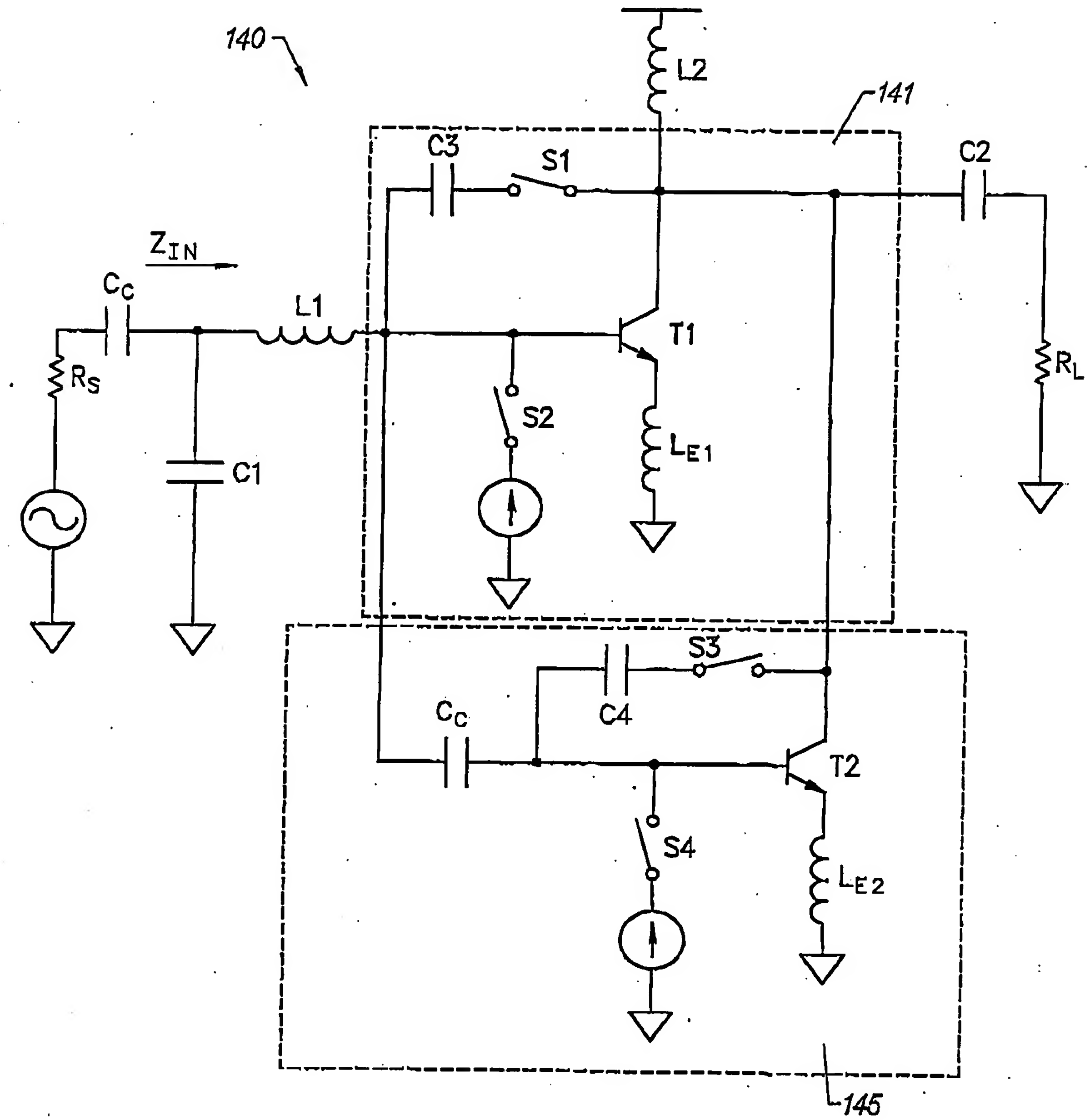
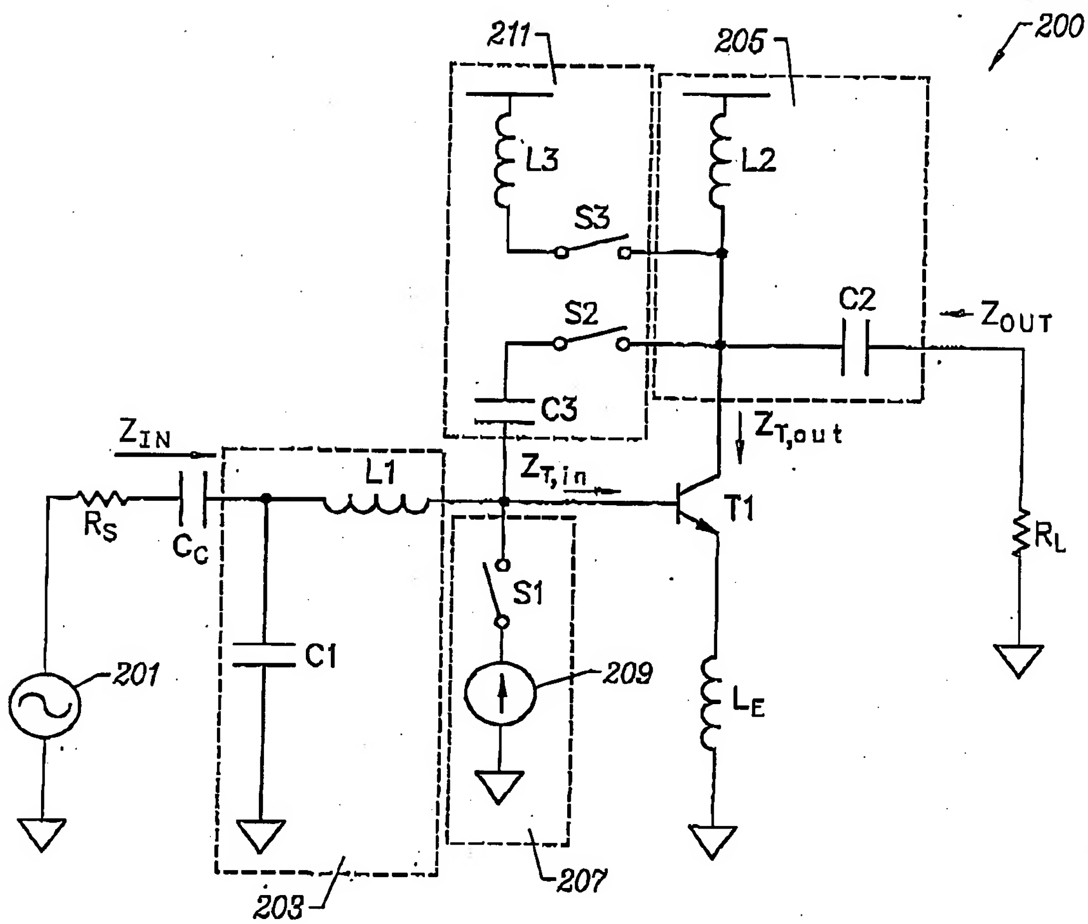



*FIG. 3*
*(PRIOR ART)*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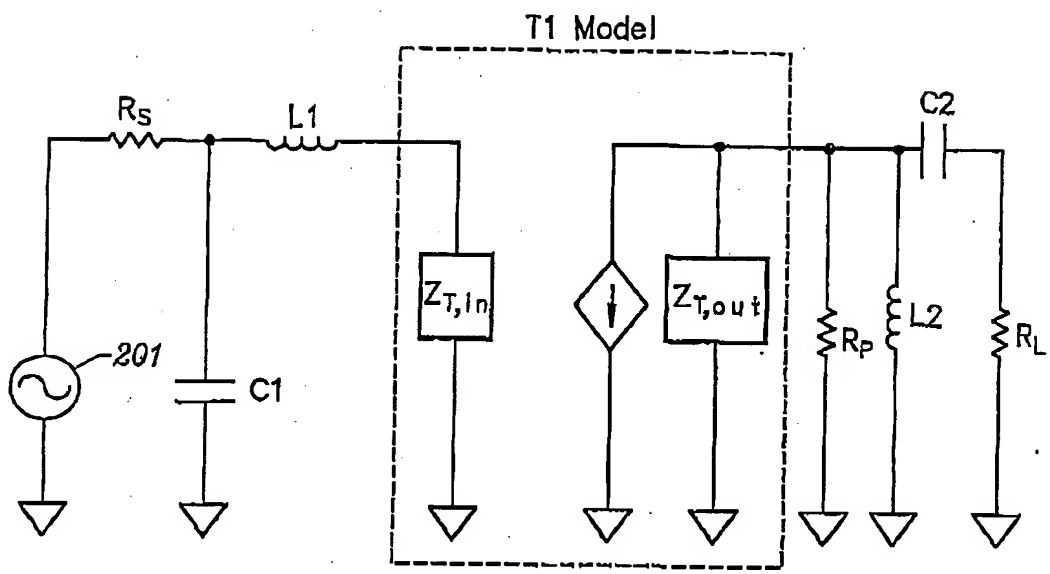
211
205
L3
L2
S3
S2
C2
ZOUT
C3
ZIN
ZT,out
L1
ZT,in
T1
RS
CC
S1
RL
C1
201
209
LE
203
207

FIG. 4


T1 Model
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L1
C2
$Z_{T,in}$
$Z_{T,out}$
$R_P$
L2
$R_L$
201
C1

FIG. 5

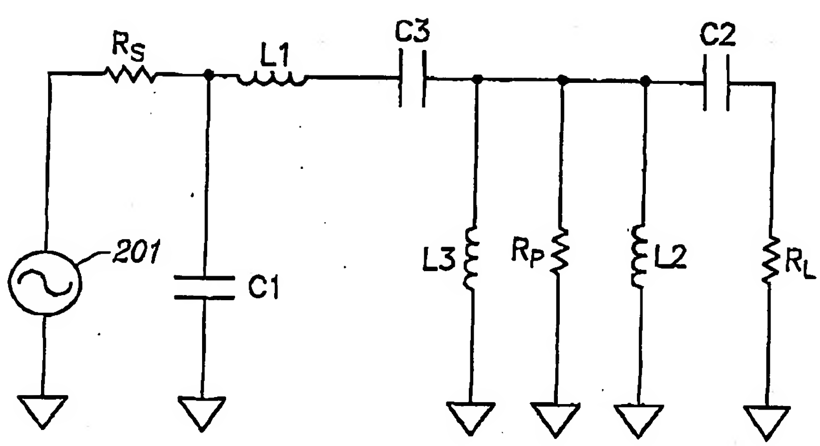

$R_S$
L1
C3
C2
201
C1
L3
$R_P$
L2
$R_L$

FIG. 6

6/12

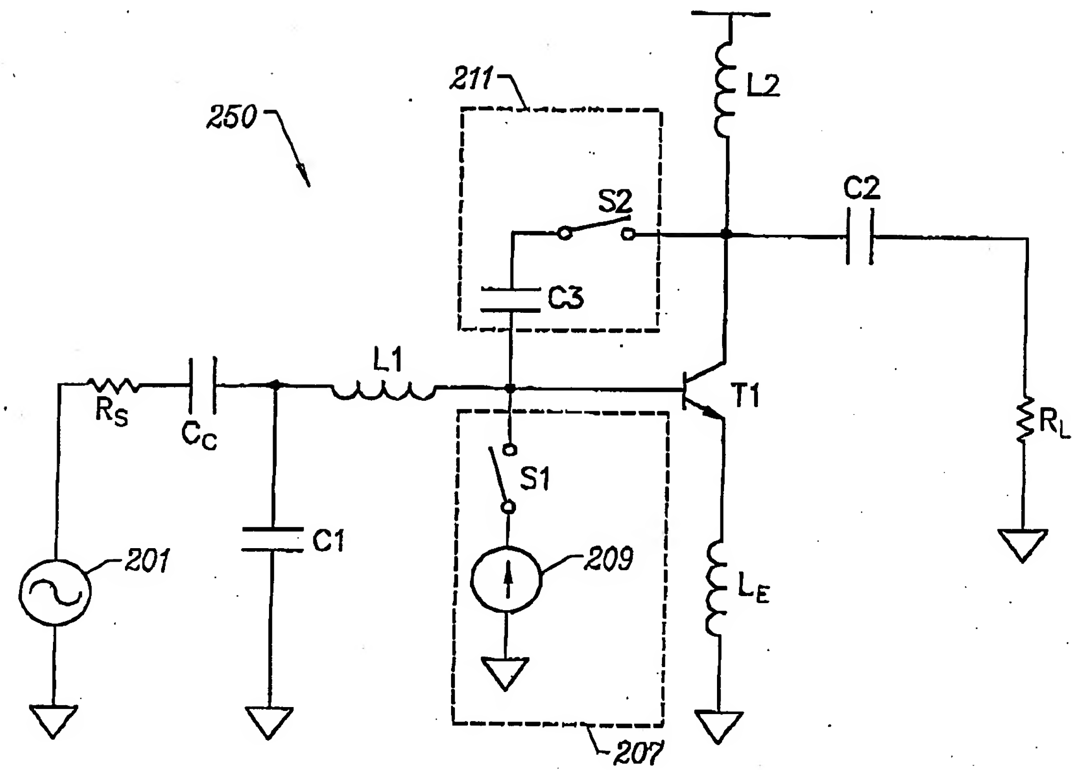



FIG. 7

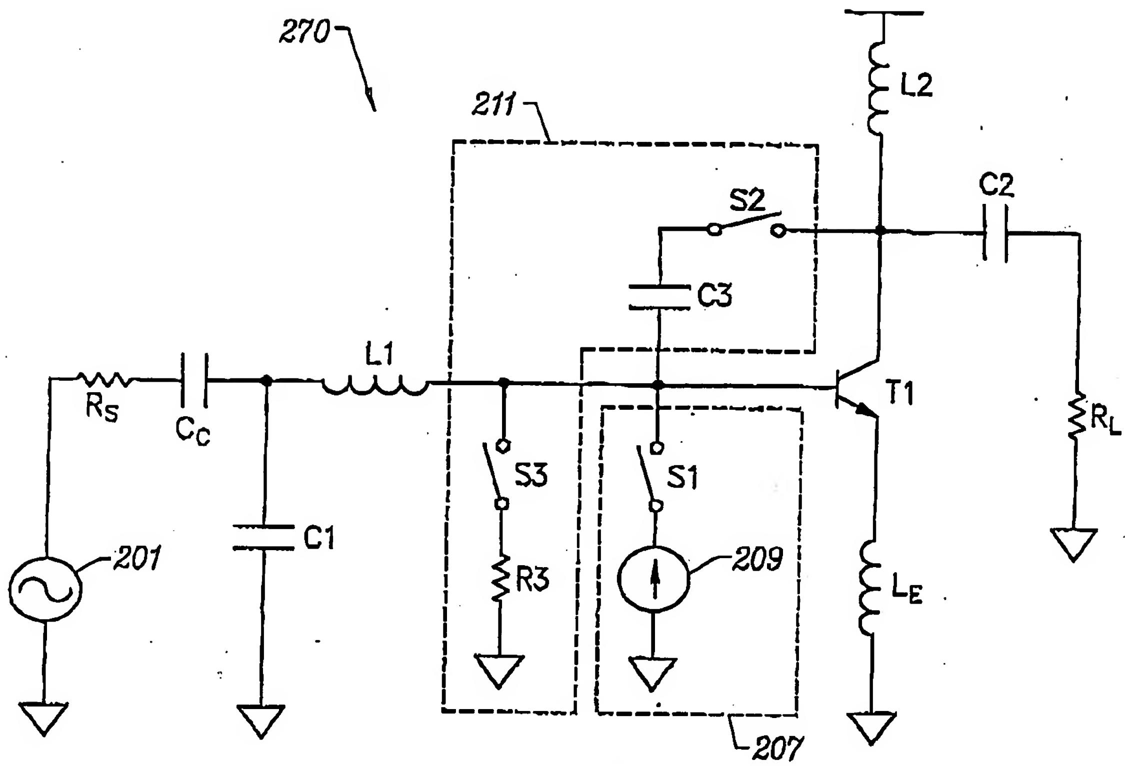



FIG. 8

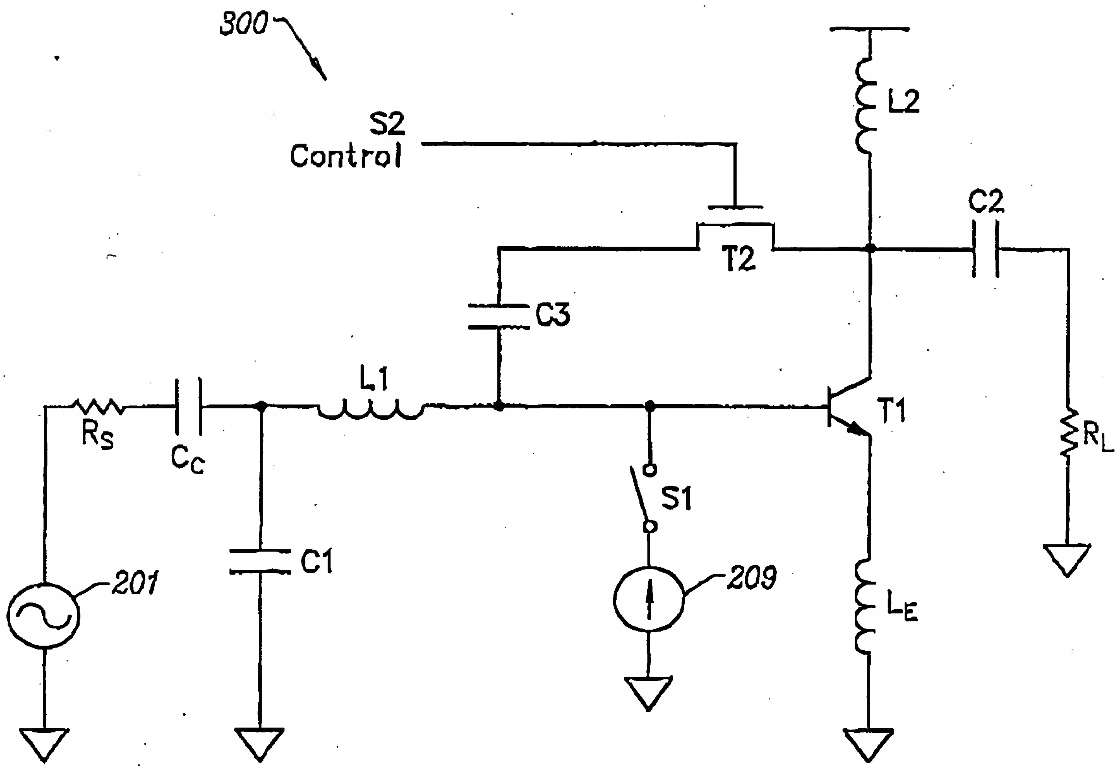



FIG. 9

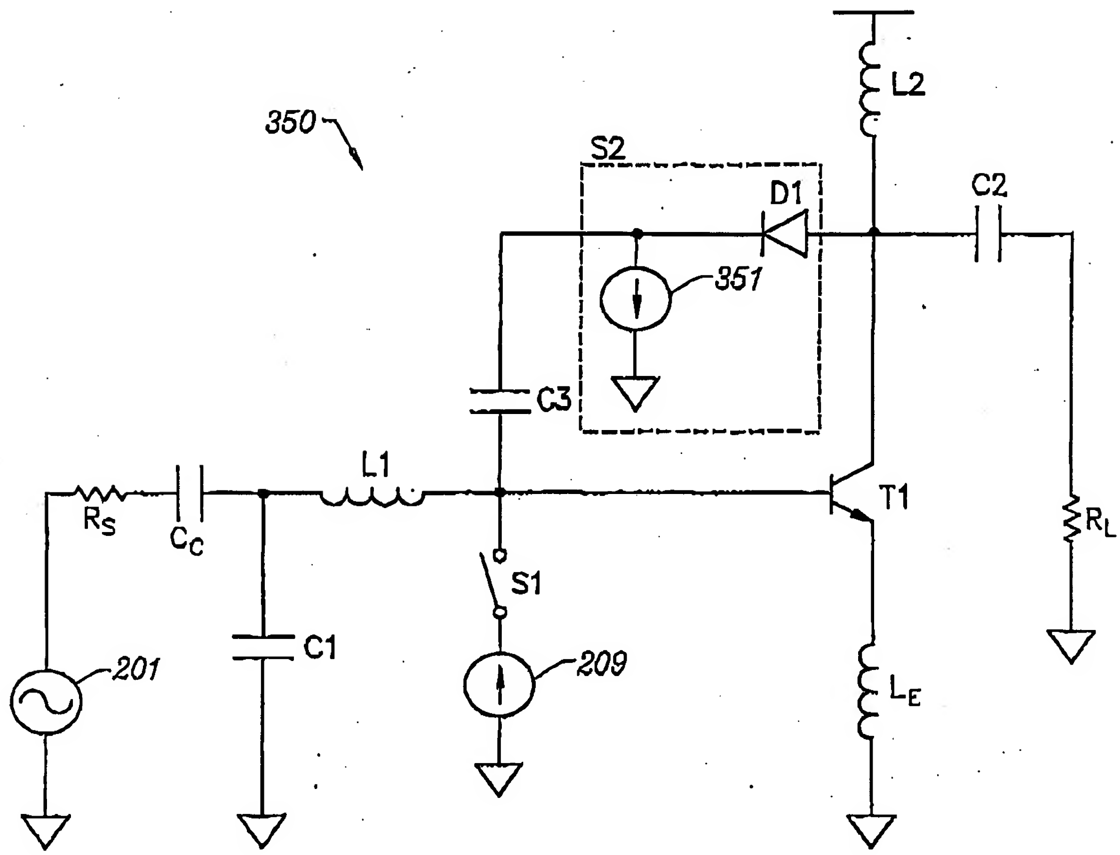
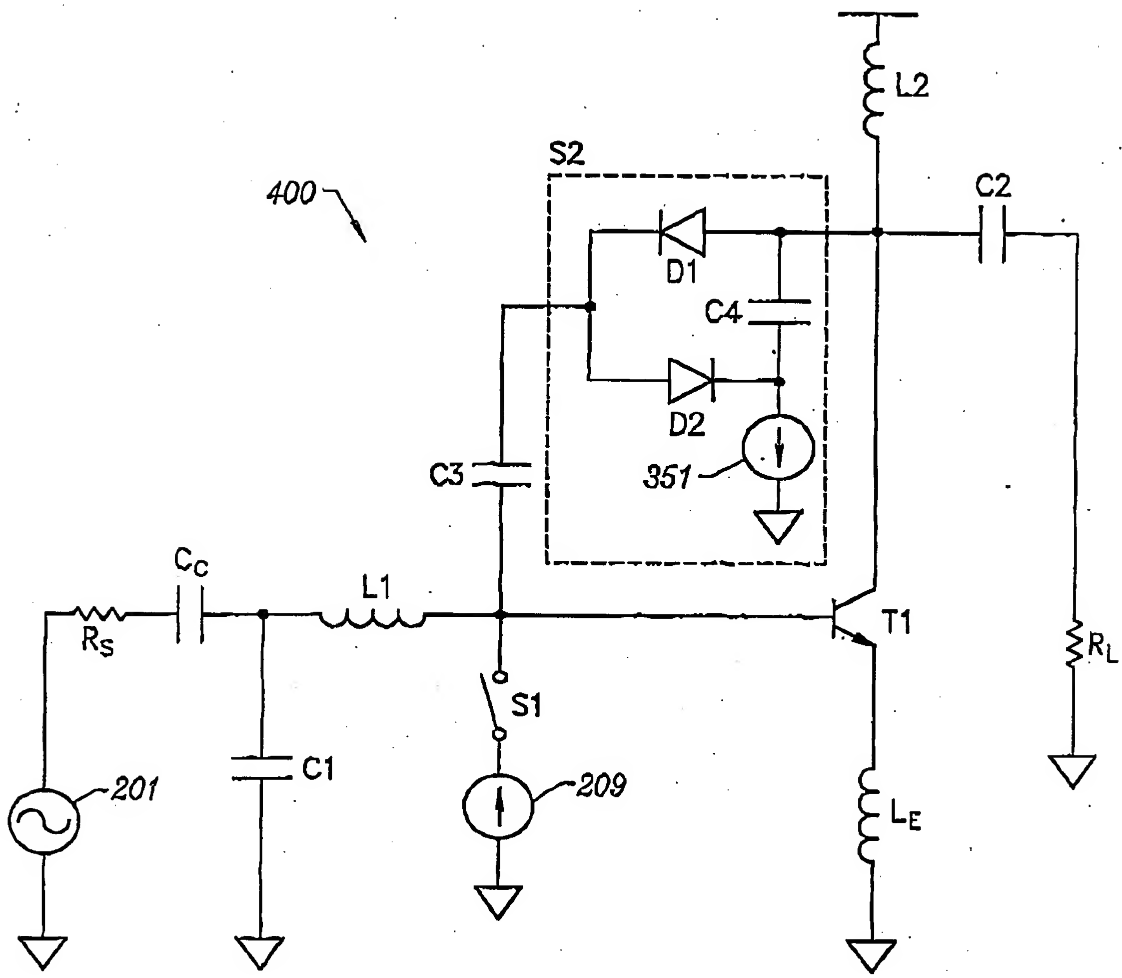
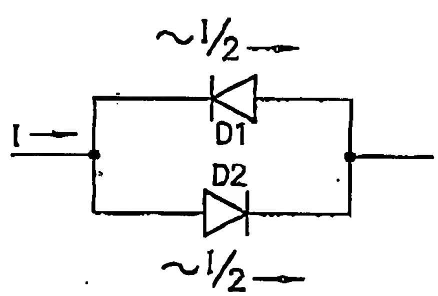



FIG. 10



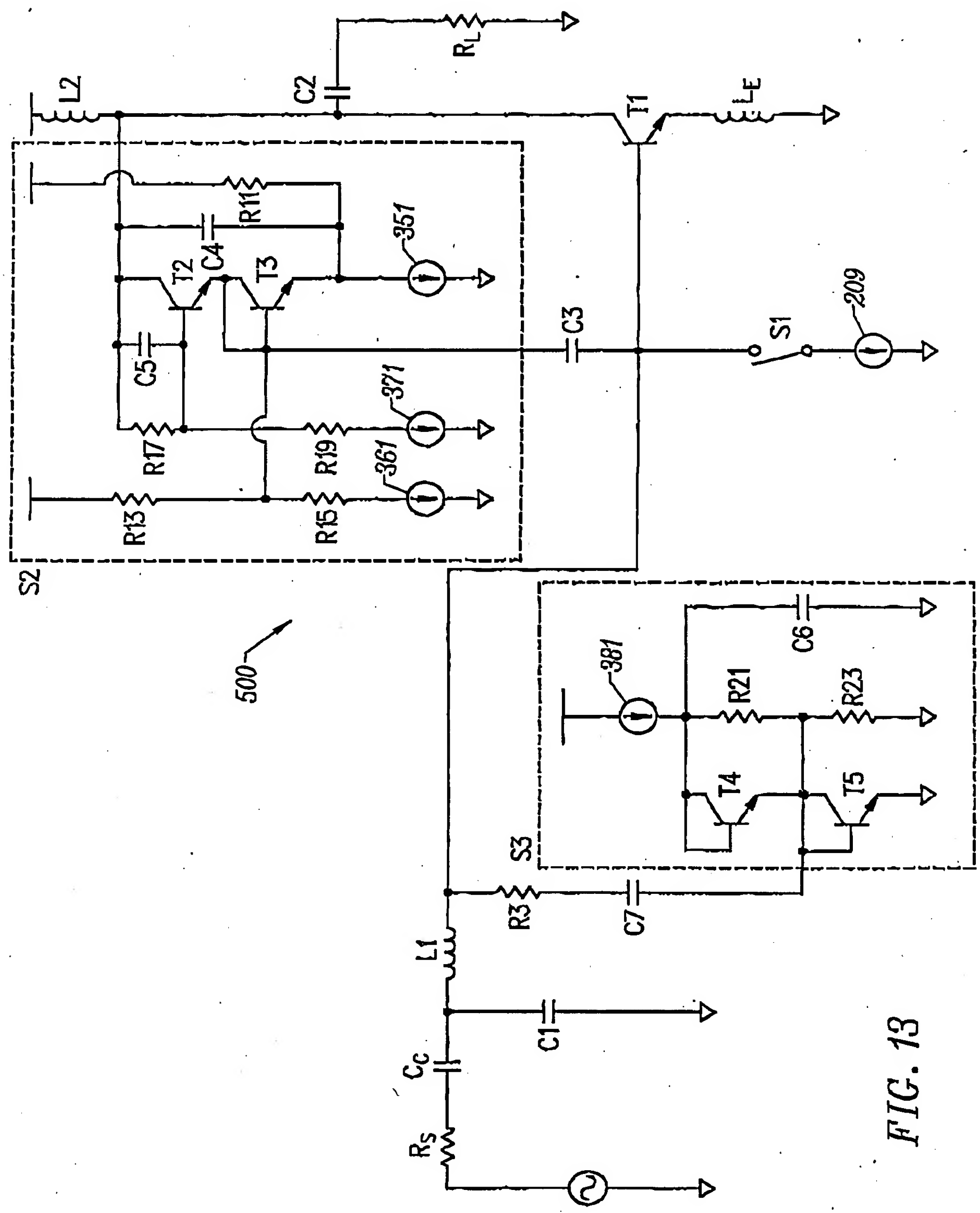
L2
S2
C2
400
D1
C4
D2
C3
351
Cc
L1
T1
RL
Rs
S1
C1
201
209
LE


FIG. 11



~I/2
I
D1
D2
~I/2


FIG. 12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C2
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T1
$L_E$
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C4
T2
T3
351
C5
C3
S1
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R19
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R13
R15
361
S2
500
381
C6
R21
R23
T4
T5
S3
R3
C7
L1
C1
$C_C$
$R_S$

FIG. 13

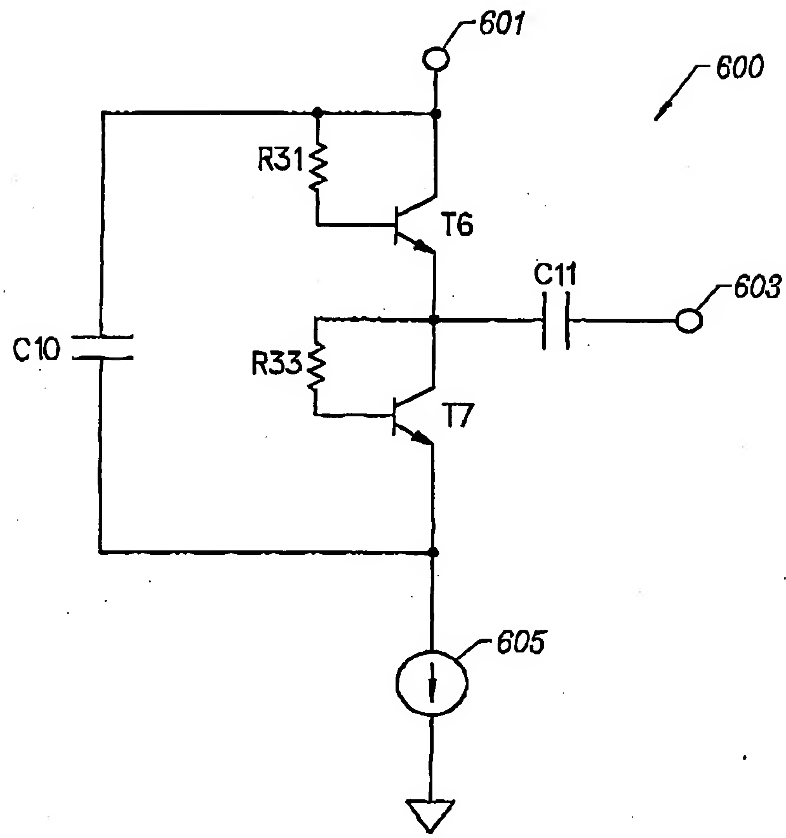


FIG. 14

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(71) Applicant *(for all designated States except US)*: MAXIM INTEGRATED PRODUCTS, INC. [US/US]; 120 San Gabriel Drive, Sunnyvale, CA 94086 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: LEE, Sheng-Hann [US/US]; 14029 Saratoga Hills Road, Saratoga, CA 95070 (US).

(74) Agent: BLAKELY, Roger, W.; Blakely, Sokoloff, Taylor & Zafman, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

(81) Designated States *(national)*: CA, US.

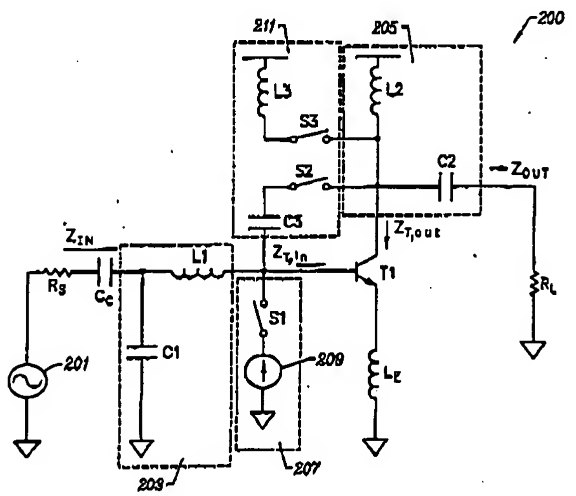
(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

**Published:**
— *with international search report*

(88) Date of publication of the international search report: 25 September 2003

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: LOW-LOSS BYPASS MODE OF AN AMPLIFIER WITH HIGH LINEARITY AND MATCHED IMPEDANCE




(57) Abstract: A switchable gain amplifier is provided. The amplifier includes an input, an output, and a first transistor having a control region, a first region, and a second region. The conduction from the first region to the second region of the first transistor is responsive to the voltage on the control region relative to the second region. An input impedance matching network is coupled with the input and the control region and an output impedance matching network is coupled with the output and the first region. A first switchable biasing circuit is coupled with the control region to switchably bias the transistor between an on state and an off state. A passive bypasse network has a firt switch to switchably couple the input impedance matching network with the output impedance matching network through the passive bypass network.

WO 02/015397 A3

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/25669

**A. CLASSIFICATION OF SUBJECT MATTER**
IPC 7 H03F3/72 H03F1/56 H03F1/02 H03G1/00 H03K17/74

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F H03G H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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| A | column 8, line 20 - line 23; figures 5-8 | 3,11-14, 17 |
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| X | US 6 043 721 A (NAGODE THOMAS DOMINIC ET AL) 28 March 2000 (2000-03-28) figure 5 | 1,2,5-8 |
| A | EP 0 837 559 A (MATSUSHITA ELECTRIC IND CO LTD) 22 April 1998 (1998-04-22) figure 17 | |

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance
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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 11 March 2003 | 10 JUN 2003 |
| **Name and mailing address of the ISA** | **Authorized officer** |
| European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016 | SEGAERT, P |

Form PCT/ISA/210 (second sheet) (July 1992)

# INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/25669

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 4 755 769 A (KATZ ALLEN) 5 July 1988 (1988-07-05) figures 2-5 | |
| A | US 4 760 363 A (GERENDT SIEGFRIED) 26 July 1988 (1988-07-26) | |

International application No.
PCT/US 01/25669

# INTERNATIONAL SEARCH REPORT

**Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)**

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-21

Remark on Protest
☐ The additional search fees were accompanied by the applicant's protest.
☐ No protest accompanied the payment of additional search fees.

International Application No. PCT/US 01/25669

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-21

   A switchable gain amplifier

2. Claims: 21-31

   a switch coupling two ports

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 01/25669

| Patent document cited in search report | | Publication date | Patent family member(s) | | Publication date |
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Form PCT/ISA/210 (patent family annex) (July 1992)